CLAIMS

We claim:

1. An arrangement comprising a first semiconductor chip and a second semiconductor chip connected thereto,

- where the second semiconductor chip is additionally connected to electrical loads and drives these electrical loads on the basis of a timing which is defined by load control data,
- where the first semiconductor chip transmits to the second semiconductor chip the load control data and pilot data which control the second semiconductor chip, and
- where the second semiconductor chip transmits to the first semiconductor chip diagnostic data which represent at least one of states prevailing in the second semiconductor chip and events which occur in the second semiconductor chip,

wherein the second semiconductor chip includes means for transmitting the diagnostic data via a first transmission channel connected between the first and second semiconductor chips, and the first semiconductor chip includes means for transmitting the load control data and the pilot data via a second transmission channel connected between the first and second semiconductor chips.

2. The arrangement as claimed in claim 1, wherein the first semiconductor chip is a program-controlled unit.

3. The arrangement as claimed in claim 1 wherein the second semiconductor chip is a power chip.

4. The arrangement as claimed in claim 1, wherein the second transmission channel comprises

- a transmission clock line via which the first semiconductor chip transmits a transmission clock signal to the second semiconductor chip,
- a data line via which the first semiconductor chip transmits the load control data and the pilot data to the second semiconductor chip in time with the transmission clock signal, and
- a chip select line via which the first semiconductor chip transmits the chip select signal to the second semiconductor chip, said chip select signal signaling to the second semiconductor chip the start and end of the transmission of data intended for the second semiconductor chip via the data line.

5. The arrangement as claimed in claim 1, wherein

the load control data and the pilot data are transmitted in units of frames, and wherein the load control data frames and the pilot data frames are transmitted using time-division multiplexing.

6. The arrangement as claimed in claim 5, wherein

the first semiconductor chip defines time windows of constant length and transmits in each time window either a load control data frame or a control data frame or no data.

7. The arrangement as claimed in claim 6,

wherein

the first semiconductor chip transmits no further load control data frame for a respective length of n time windows after transmission of a load control data frame, where $n \geq 0$ and where n can be set by the user of the arrangement.

8. The arrangement as claimed in claim 7, wherein

a pilot data frame can be transmitted only in a time window in which no load control data frame is to be transmitted.

9. The arrangement as claimed in claim 6, wherein

transmission of the pilot data has priority when load control data and pilot data are awaiting transmission simultaneously.

10. The arrangement as claimed in claim 1, wherein

the first transmission channel comprises a data line, and wherein this line is used to transmit neither load control data nor pilot data.

11. The arrangement as claimed in claim 1, wherein

the diagnostic data are transmitted in time with a transmission clock signal generated in the second semiconductor chip, and wherein this transmission clock

signal is not transmitted to the first semiconductor chip.

12. The arrangement as claimed in claim 1, wherein

the first semiconductor chip transmits appropriate pilot data in order to prescribe to the second semiconductor chip what transmission rate is to be used by the second semiconductor chip to transmit the diagnostic data to the first semiconductor chip.

13. The arrangement as claimed in claim 12, wherein

the transmission rate is prescribed by transmitting a division factor, and wherein the second semiconductor chip divides the frequency of a transmission clock signal transmitted to it by the first semiconductor chip by the division factor and transmits the diagnostic data to the first semiconductor chip in time with the resultant signal.

14. The arrangement as claimed in claim 13, wherein

the transmission clock signal supplied to the second semiconductor chip represents the transmission clock which is used by the first semiconductor chip to transmit the load control data or the pilot data to the second semiconductor chip.

15. The arrangement as claimed in claim 11, wherein

the diagnostic data are transmitted in units of frames, where a frame starts with a start bit having a prescribed value and ends with one or two stop bits having prescribed values.

16. The arrangement as claimed in claim 11, wherein

the first semiconductor chip ascertains the phase of the diagnostic data by oversampling the diagnostic data.

17. The arrangement as claimed in claim 1, wherein

the first transmission channel comprises a transmission clock line via which the first semiconductor chip transmits a transmission clock signal to the second semiconductor chip, or the second semiconductor chip transmits a transmission clock signal to the first semiconductor chip, and wherein the second semiconductor chip transmits the diagnostic data in time with this transmission clock signal.

18. The arrangement as claimed in claim 1, wherein

the second transmission channel comprises

- a first transmission clock line via which the first semiconductor chip transmits a transmission clock signal to the second semiconductor chip,
- a second transmission clock line via which the first semiconductor chip transmits the inverse transmission clock signal to the second semiconductor chip,
- a first data line via which the first semiconductor chip transmits the load control data and the pilot data to

the second semiconductor chip in time with the transmission clock signal,

- a second data line via which the first semiconductor chip transmits the inverse load control data and the inverse pilot data to the second semiconductor chip, and
- a chip select line via which the first semiconductor chip transmits a chip select signal to the second semiconductor chip, said chip select signal signaling to the second semiconductor chip the start and end of the transmission of data intended for the second semiconductor chip via the data line.

19. The arrangement as claimed in claim 18, wherein

the output drivers on the first semiconductor chip, which output the load control data, the pilot data and the transmission clock signal, are LVDS drivers or other special drivers whose use limits electromagnetic interference.

20. The arrangement as claimed in claim 1, wherein

the first semiconductor chip has a plurality of respective different output drivers for outputting the load control data, the pilot data and the transmission clock signal, and wherein the user of the arrangement is able to set which of the plurality of different output drivers needs to be used in each case.

21. The arrangement as claimed in claim 5, wherein

the first semiconductor chip is connected to a plurality of second semiconductor chips, and wherein a first portion of the data transmitted in a frame is intended for a first second semiconductor chip, and a second portion of the data transmitted in this frame is intended for a second semiconductor chip.

22. The arrangement as claimed in claim 5, wherein

- the first semiconductor chip is connected to a plurality of second semiconductor chips,
- every second semiconductor chip is connected to the first semiconductor chip via a dedicated chip select line, and
- the chip select signals transmitted via the chip select lines can be altered during the transmission of a frame.